REMARKS

Applicant requests reconsideration and withdrawal of the rejections set forth in the above-mentioned Office Action, in view of the foregoing amendments and the following remarks.

Claims 1, 3-6, and 8-18 remain pending in this application, with Claim 1 being the sole independent claim. By this Amendment, Applicant has cancelled Claim 7, and amended Claim 1.

Claims 1, 3-6, and 8-18 stand rejected under 35 U.S.C. § 103 as being unpatentable over U.S. Patent Publication No. 2004/0042705 A1 (Uchida, et al.) in view of Applicant's own disclosure and U.S. Patent No. 4,267,587 (Mizuno, et al.). Claim 7 stands rejected under 35 U.S.C. § 103 as being unpatentable over Uchida, et al. in view of Applicant's own disclosure and U.S. Patent No. 4,845,702 (Melindo). Applicant traverses these rejections.

As recited in independent Claim 1, Applicant's invention is directed to an optical waveguide device. The device includes a slab-type optical waveguide layer and a plurality of chips which include optical input and output ports for inputting and outputting an optical signal. An optical input port receives an optical signal, output by an optical output port, in accordance with a timing control signal inputted using an electrical connection between the plurality of chips. The timing control signal is an electrical signal obtained by dividing a clock frequency for the optical signal. Further, the optical signal output by the optical output port comprises a packet signal train formed of a finite pulse train, and the timing control signal is individually sent as an instruction signal used to select adoption or rejection of the packet signal

to carry out time division packet switching, in order to switch an optical connection between the optical input and output ports.

The Office Action cites Uchida, et al. as describing an optical waveguide (although not a slab-type optical waveguide) and electrical wiring for interconnecting various components. Mizuno, et al. is cited as describing an electric clock with a frequency divider and components for producing different types of timing and control signals. Melindo is cited in the Office Action as teaching high-speed packet switching in a network.

It is the position set forth in the Office Action that the separate descriptions in various references of optical and electrical signals, a timing control signal using a divided clock frequency, and packet signal trains would lead one of ordinary skill in the art to arrive at the present invention. However, Applicant submits that the mere disclosure of the existence of these different types of signals and transmission mechanisms does not suggest the recited features of the present invention.

In particular, the present invention is directed to a combination of optical and electrical signals in which a timing control signal is an electrical signal obtained by dividing a clock frequency for the optical signal, and the optical signal comprises a packet signal train, with the timing control signal being individually sent as an instruction signal used to select adoption or rejection of the packet signal to carry out time division packet switching to switch an optical connection between input and output ports. Thus, the invention is generally directed to a mechanism for using a combination of an optical signal transmitting information and an electrical signal used for packet control to provide a novel optical switching system. Applicant

submits that this switching mechanism is not rendered obvious merely by the existence of individual references variously discussing optical, electrical, and clock signals. Moreover, Applicant submits that the Office Action does not provide a discussion of the specific motivation provided in one more of the references to combine them in a manner which would achieve the switching mechanism recited in independent Claim 1.

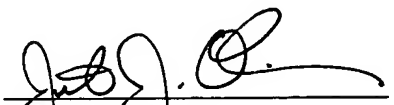
Accordingly, Applicant submits that Uchida, et al., Mizuno, et al., and Melindo, taken alone or in combination, fail to disclose or suggest at least the features of optical input and output ports for inputting and outputting an optical signal to and from a slab-type optical waveguide layer, wherein the optical input port receives an optical signal from the optical output port in accordance with a timing control signal, wherein the timing control signal is an electrical signal obtained by dividing a clock frequency for the optical signal, and wherein the optical signal comprises a packet signal train formed of a finite pulse train, with the timing control signal being individually sent as an instruction signal used to select adoption or rejection of the packet signal to thereby switch an optical connection between the optical input and output ports, as recited in independent Claim 1.

Applicant submits that the dependent claims are allowable, in their own right, for defining features of the present invention in addition to those recited above with respect to independent Claim 1. Applicant requests individual consideration of the dependent claims.

For the foregoing reasons, Applicant requests withdrawal of the rejections under 35 U.S.C. § 103.

Applicant's undersigned attorney may be reached in our Washington, D.C. office by telephone at (202) 530-1010. All correspondence should continue to be directed to our address given below.

Respectfully submitted,



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